WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming an isolation groove between a plurality of active regions in a first major surface of a wafer;

(b) forming an insulating region in the isolation groove by depositing an insulating layer;

(c) synthesizing water vapor from oxygen and hydrogen gases by use of a catalyst;

(d) keeping the thus synthesized water vapor in a gaseous state and feeding it into a processing chamber to form a wet oxidative atmosphere;

(e) after step (b), performing thermal oxidation treatment to a silicon surface portion over one of the active regions to form an insulating film under the wet oxidative atmosphere in the processing chamber.

2. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein said wet oxidative atmosphere includes oxygen gas as a principal oxidative gas component.

3. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein said wet oxidative atmosphere includes oxygen gas as a principal gas component.

4. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

5. A method for fabricating a semiconductor integrated circuit device according to Claim 4, wherein the gate length of said insulated gate field effect transistor is not more than 0.25 μm.

6. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein planarization is performed by removing the insulating layer outside the isolation groove between steps (b) and (e).

7. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein the planarization is performed by a chemical mechanical method.

8. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein the planarization is performed by a chemical mechanical polishing.

9. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein the deposition of the insulating layer is performed by chemical vapor deposition.

10. A method for fabricating a semiconductor integrated circuit device

according to Claim 1, wherein a temperature of the thermal oxidation is not lower than 800°C.

11. A method for fabricating a semiconductor integrated circuit device according to Claim 1, wherein the thermal oxidation is performed while feeding said oxidative atmosphere over the first major surface of said wafer.

12. A method for fabricating a semiconductor integrated circuit device according to Claim 2, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

13. A method for fabricating a semiconductor integrated circuit device according to Claim 3, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

14. A method for fabricating a semiconductor integrated circuit device according to Claim 5, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

15. A method for fabricating a semiconductor integrated circuit device according to Claim 6, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

16. A method for fabricating a semiconductor integrated circuit device according to Claim 7, wherein the gate insulating film is a gate insulating film of an

insulated gate field effect transistor.

17. A method for fabricating a semiconductor integrated circuit device according to Claim 8, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

18. A method for fabricating a semiconductor integrated circuit device according to Claim 9, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

19. A method for fabricating a semiconductor integrated circuit device according to Claim 11, wherein the gate insulating film is a gate insulating film of an insulated gate field effect transistor.

20. A method for fabricating a semiconductor integrated circuit device according to Claim 6, wherein the gate length of said insulated gate field effect transistor is not more than 0.25 μm.

21. A method for fabricating a semiconductor integrated circuit device according to Claim 7, wherein the gate length of said insulated gate field effect transistor is not more than 0.25 μm.

22. A method for fabricating a semiconductor integrated circuit device according to Claim 8, wherein the gate length of said insulated gate field effect transistor is not more than 0.25 μm.

23. A method for fabricating a semiconductor integrated circuit device according to Claim 9, wherein the gate length of said insulated gate field effect transistor is not more than 0.25 μm.

24. A method for fabricating a semiconductor integrated circuit device according to Claim 11, wherein the gate length of said insulated gate field effect transistor is not more than 0.25 μm.

25. A method for fabricating a semiconductor integrated circuit device according to Claim 7, wherein planarization is performed by removing the insulating layer outside the isolation groove between steps (b) and (e).

26. A method for fabricating a semiconductor integrated circuit device according to Claim 8, wherein planarization is performed by removing the insulating layer outside the isolation groove between steps (b) and (e).

27. A method for fabricating a semiconductor integrated circuit device according to Claim 9, wherein planarization is performed by removing the insulating layer outside the isolation groove between steps (b) and (e).

28. A method for fabricating a semiconductor integrated circuit device according to Claim 11, wherein planarization is performed by removing the insulating layer outside the isolation groove between steps (b) and (e).

29. A method for fabricating a semiconductor integrated circuit device according to Claim 9, wherein the planarization is performed by a chemical mechanical method.

30. A method for fabricating a semiconductor integrated circuit device according to Claim 11, wherein the planarization is performed by a chemical mechanical method.

31. A method for fabricating a semiconductor integrated circuit device according to Claim 9, wherein the planarization is performed by chemical mechanical polishing.

32. A method for fabricating a semiconductor integrated circuit device according to Claim 11, wherein the planarization is performed by chemical mechanical polishing.

33. A method for fabricating a semiconductor integrated circuit device according to Claim 11, wherein the deposition of the insulating layer is performed by chemical vapor deposition.